IN THE CLAIMS

Please cancel Claims 8-18 without prejudice or disclaimer.

Please amend Claims 1, 19, and 22-29 as follows:

Sub B17

1. A post-processing method for use in a sampled data read channel of a mass data storage device that has a Viterbi detector that receives actual sampled partial response target data from a data medium of said mass data storage device and produces a recovered data output signal, comprising:

filtering a recovered partial response target signal derived from said recovered data output signal and sampled partial response target data to produce a filtered output signal;

providing a threshold circuit to provide a threshold against which said filtered output signal is compared;

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generating an error event pattern indicating signal when a predetermined error event pattern occurs in said recovered data output signal;

modifying the recovered data output signal when said filtered output signal exceeds the threshold of said threshold circuit and said error event indicating signal is generated, and

whitening the recovered data output signal, prior to said filtering but within said port processing method, with a whitening filter.

19. A post-processor circuit for use in a sampled data read channel of a mass data storage device, comprising:

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a Viterbi detector that receives an actual sampled partial response target signal from a storage medium of said mass data storage device to produce a recovered data output signal;

an error pattern detector to generate an error pattern event indicating signal if a predetermined error event pattern occurs in said sampled partial response target signal;

a circuit for generating an error signal based upon a difference between said recovered data output signal and a delayed said actual sampled partial response target signal;

a threshold circuit to generate an error correction control signal if a magnitude of said error signal exceeds a predetermined threshold;

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an error correction circuit to modify the recovered data output signal when said error correction control signal and said error event pattern indicating occurrence signal are generated, and

a whitening filter connected to receive said error signal to produce an input signal to said threshold circuit.

22. The circuit of Claim 19 wherein said predetermined error pattern event is ex = ±{1}.

23. The circuit of Claim 19 wherein said predetermined error pattern event is ex = ±{1-11}.

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24. The circuit of Claim 19 wherein said predetermined error pattern event is ex = ±{1-1}.

25. The circuit of Claim 19 wherein said circuit for generating an error signal is an FIR filter.

26. The circuit of Claim 19 wherein said circuit for generating an error signal is an error pattern matched filter.

27. The circuit of Claim 19 wherein said circuit for generating an error signal comprises a whitening noise generator and an FIR filter connected to receive an output of said whitening noise generator.

28. The circuit of Claim 19 wherein said Viterbi detector has a partial response level of at least EPR4.

29. The circuit of Claim 19 wherein said Viterbi detector has a partial response level of at least EEPR4.